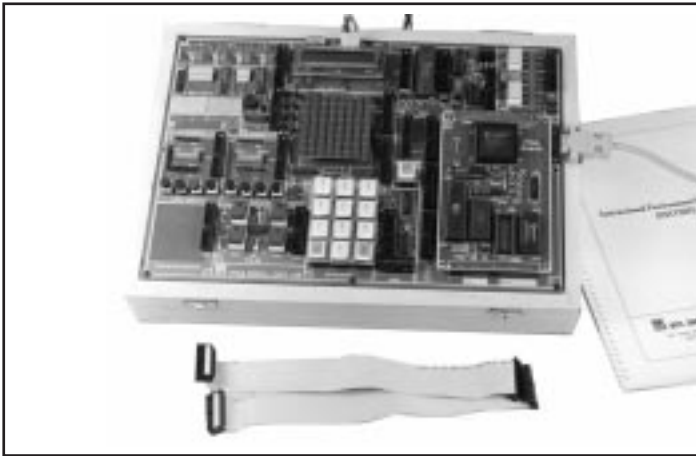


FPGA DIGITAL LOGIC LAB-I

FPGA Trainer (Technical know-how from IIT, Delhi)

FPGA DIGITAL LOGIC LAB-II**FEATURES**

- Field Programmable Gate Array Trainer commonly known as FPGA Trainer uses industrial standard **Xilinx FPGA 3142**.
- It has level microcontroller 8051 family processor to enable it to upload and download program to/from FPGA.
- It has a serial link which enables user to communicate with PC at a standard baud rate.
- User can develop the circuit/schematic using Xilinx standard Foundation Series Software.
- It has an **INCODE Software** to enable user to:
 - Download Program
 - Upload Program
 - Run Program
 - Upload Data from RAM into a file
 - Download Data from a file onto the RAM
 - Register Setting
 - Download Configuration
 - Download FPGA data
 - Download FPGA Data from a file
 - Upload FPGA Data
 - Upload FPGA Data to file
 - Diagnostic Mode
 - Settings
- It has I/O counter interface to enable it to connect to various demo modules. This helps in man to machine interface.
- System has 64K byte of EPROM & 32K byte of RAM.
- All the pin outs of FPGA are available on the board. This helps in man - machine interface.

SPECIFICATIONS

- Supported chip: Xilinx 3142 on board experiments.
- **Signal generation unit:**
 1. Programmable frequency generator
 2. Standard frequency 1/10/100/1K/10K/100K/1M/10MHz
- **Logic input switch:**
 1. 8 x 1 logic input original press point with light
 2. 8 x 2 logic input Dip switch
 3. 4 impulse press button generator (2 positive pulse 2 negative pulse)
- **Output unit:**
 1. 8 x 8 of matrix (LED) display
 2. 2 x 3 seven segment display

3. 16 x 1 LCD display
4. 1 set buzzer output
5. 1 x 4 and 1 x 8 bar code output
6. 12 x 1 LED display to perform traffic light experiment

 Linear unit:

1. 1 set 8 bit D/A converter
2. 1 set 8 bit A/D converter

 MPU unit:

8051 operations

 Library Components:

In order to facilitate a smooth operation for the user who, wish directly go ahead with their designs.

1. Bounce Eliminator
2. PC Interfacing Module (PC Input/Output)
3. PC Interfacing Module (PC RAM)
4. Up-down Counter
5. Sequential Divider
6. First in First out Buffer (FIFO)
7. Hamming Distance Calculator
8. Incrementor
9. Last in First Out Buffer (LIFO)
10. L.C.D. Interface
11. DAC Interface
12. ADC Interface
13. Keyboard Interface
14. 8 x 8 LED Matrix
15. Seven Segment

 Case Studies:

- | | |
|------------------|--------------------|
| 1. FIFO Unit | 2. Ping Pong Unit |
| 3. Stack Machine | 4. Hardware Sorter |

THEMATIC APPLICATION TEST

- 8 x 8 LED control test
- Counter
- Keyboard scan
- LCD display control test
- A/D, D/A converter test
- Easy CPU design
- Matching 8051 thematic test
- Stepper motor driver design

APPLICATION PROGRAM RANGE

1. Fundamental logic program
2. Digital circuit design program
3. Digital system design circuit program
4. Micro processor principle program
5. VLSI design program
6. CPLD/FPGA chip design program
7. 8051 single chip program
8. Thematic preparation

ELECTRICAL SPECIFICATION

- 220V, 50HZ AC INPUT
- SERIAL PORT DOWNLOAD INTERFACE

FPGA DIGITAL LOGIC LAB-II
FPGA Trainer

- Uses industrial standard **Xilinx FPGA 4010**.

Note: Specifications can be changed and added without notice in our constant efforts for improvement.



FEATURES

- Field Programmable Gate Array Trainer commonly known as FPGA Trainer uses industrial standard **Xilinx FPGA 3142**.
- It has level microcontroller 8051 family processor to enable it to upload and download program to/from FPGA.
- It has a serial link which enables user to communicate with PC at a standard baud rate.
- User can develop the circuit/schematic using Xilinx standard Foundation Series Software.
- It has Software to enable user to Download Program, Upload Program, Run Program, Upload Data from RAM into a file, Download Data from a file onto the RAM, Register Setting, Download Configuration, Download FPGA data, Download FPGA Data from a file, Upload FPGA Data, Upload FPGA Data to file, Diagnostic Mode, Settings etc.
- It has I/O counter interface to enable it to connect to various demo modules. This helps in man to machine interface.
- System has 64K byte of EPROM & 32K byte of RAM.
- All the pin outs of FPGA are available on the board. This helps in man - machine interface.**

SPECIFICATIONS

- Supported chip: Xilinx 3142 on board experiments.
- **Logic input switch:**
 1. 8 x 1 logic input original press point with light
 2. 8 x 2 logic input Dip switch
- **Output unit:**
 1. 2 x 3 seven segment display
 2. 12 x 1 LED display to perform traffic light experiment
- **Linear unit:**
 1. 1 set 8 bit D/A converter
 2. 1 set 8 bit A/D converter

● Library Components:

In order to facilitate a smooth operation for the user who wish directly go ahead with their designs (without wanting to go in more detailed aspects of peripheral devices) software module of almost all peripheral devices have been added as library components. These are: Bounce Eliminator, PC Interfacing Module (PC Input/Output), PC Interfacing Module (PC RAM), Up-down Counter, Sequential Divider, First in First out Buffer (FIFO), Hamming Distance Calculator, Incrementor, Last in First Out Buffer (LIFO), DAC Interface, ADC Interface, 8 x 8 LED Matrix, Seven Segment etc.

APPLICATION PROGRAM RANGE

1. FUNDAMENTAL LOGIC PROGRAM
2. DIGITAL CIRCUIT DESIGN PROGRAM
3. DIGITAL SYSTEM DESIGN CIRCUIT PROGRAM
4. MICRO PROCESSOR PRINCIPLE PROGRAM
5. VLSI DESIGN PROGRAM
6. CPLD/FPGA CHIP DESIGN PROGRAM
7. 8051 SINGLE CHIP PROGRAM
8. THEMATIC PREPARATION

ELECTRIC SPECIFICATION

- 220V, 50HZ AC INPUT
- SERIAL PORT DOWNLOAD INTERFACE

VPL-FPGA-II FPGA Trainer

- Uses industrial standard **Xilinx FPGA 4010**.
- All other specifications are same as of VPL-FPGA-I.**

Note: Specifications can be changed and added without notice in our constant efforts for improvement.

VPL-PLDT**PAL Trainer****SPECIFICATIONS**

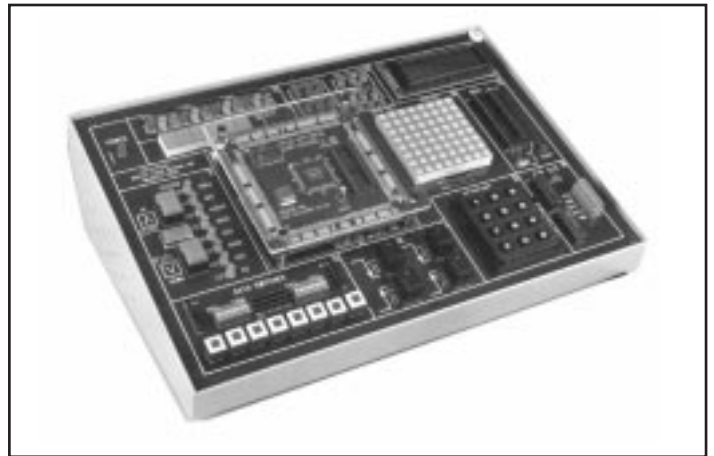
The unit is divided into two parts:

- Programmer for various GAL's
- Experimental modules for various GAL's

Experimental modules incorporate following features:

- Signal Generator: to provide signal (Sine Wave) as an input to GALs.
 - Two independent frequency output: 1Hz & 10KHz.
 - One independent adjustable clock generator: 1Hz - 1KHz.
- Switches to provide ON/OFF input to GALs.
 - Eight independent input switches
 - Each switch provides "switch - debouncing" circuit.
 - Fan out: 20 TTL loading
- Pulse Signal Switch:
 - Provides Q/R output, pulse width may be controlled manually.
 - Offers switch debouncing circuit
 - Fan out: 10 TTL loading
- Display:
 - Logic Indicator:
 - 8 independent LED to show high/low levels
 - LED indicator for DICE circuit
 - Number of Display:
 - 5 x 7 dot matrix character display (38.3 x 53.0 mm.
 - 4 independent seven segment displays
- 4 ZIF sockets (24 pins)
- Demo functions:
 - 24 hour clock (seven segment)
 - DICE (LED)
 - Neon (LED)
 - Character (dot matrix)
- Experiment types include combinational and sequential circuit experiments
- Power Supply:
 - Internal from PC: accord with PCPET Card plug in to free ISA slot of IBM compatible PC.
 - External Power Supply (optional)
- 37 Pin D type connector (connection between PCPET card main unit)

Note: Specifications can be changed and added without notice in our constant efforts for improvement.

LP-2900**CPLD/FPGA Design Experimental Kit****SPECIFICATIONS**

- Supported chip:** ALTERA FLEX10K (TQFP 144pin), employs modular design, flexibly replace with other brand CPLD or FPGA.
- Signal generation unit:**
 - Programmable frequency generator
 - Standard frequency 1/10/100/1K/10K/100K/1M/10MHz
- Logic input switch:**
 - 8 x 1 logic input original press point with light
 - 8 x 2 logic input Dip switch
 - 4 impulse press button generator (2 positive pulse 2 negative pulse)
 - 3 x 4 array keyboard.
- Output unit:**
Logic status monitor with total 102 sets LED indicator for logic status.
- 8 x 8 dual color point array LCD display.
 - LCD 16 x 2 monitor
 - 6 digits 7 nodes monitor
 - 3 x 4 LED output
 - 1 set buzzer output
- Linear unit:**
 - 2 sets 8 bit D/A converter
 - 1 set 8 bit A/D converter
- MPU unit:**
8051 and CPLD/FPGA match circuit test.

TEST CONTENT

- Combined logic design, simulation and test:
 - Basic logic
 - Deductor
 - Decoder
 - Combined logic
 - Comparator
 - Multiplexer
 - Adder
 - Compiler
 - Demultiplexer
- Sequential logic circuit design, simulation and test:
 - Flip-flop device
 - Shift register
 - Shift counter register
 - Synchronized counter
 - Non-Synchronized counter
- Analog logic circuit design, simulation and test:
 - A/D converter
 - D/A converter

ELECTRICAL SPECIFICATION

- AC90-260V, 50/60HZ AC input
- Print port down load interface